UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/942,102	08/29/2001	William R. Wheeler	10559-595001 / P12879	6907

20985 7590 03/31/2003

FISH & RICHARDSON, PC
4350 LA JOLLA VILLAGE DRIVE
SUITE 500
SAN DIEGO, CA 92122

EXAMINER
THOMPSON, ANNETTE M

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 03/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/942,102	WHEELER ET AL.	
	Examin r	Art Unit	
	A. M. Thompson	2825	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,10-16,20-26 and 30* is/are rejected.

7)☒ Claim(s) *7-9,17-19 and 27-29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This application 09/942,102, has been examined. Claims 1-30 are pending.

Claim Objections

1. **Claims 8, 9, 19, 28, 29** are objected to because of the following informalities: Pursuant to claims 8 and 28, end the claims with a period. Pursuant to claims 9, 19, and 29, at line 2, change "presentation" to –representation--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Rejection of claims 1-6, 10-16, 20-26 and 30

3. Claims 1-6, 10-16, 20-26 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Rostoker et al. (Rostoker), U.S. Patent 5,544,067. Rostoker teaches a system for interactive design, synthesis and simulation of an electronic system allowing a user to design a system by specification of a behavioral model in a high level language such as VHDL or by graphical entry.

4. Pursuant to claim 1, which recites [a] method of generating a logic design (col. 12, ll. 40-4) for use in designing an integrated circuit comprising embedding a combinatorial one-dimensional logic block representing a combinatorial element within a

two-dimensional schematic representation of the logic design to produce a unified database representation of the logic design (col. 26, ll. 4-16).

5. Pursuant to claim 2, further comprising generating the combinatorial one-dimensional logic block (col. 27, ll. 19-40).

6. Pursuant to claim 3, further comprising importing the combinatorial one-dimensional logic block (col. 27, ll. 34-42).

7. Pursuant to claim 4, further comprising following a set of design capture rules (col. 27, line 59 to col. 28, line 17).

8. Pursuant to claim 5, further comprising notifying a designer when capturing data violates the set of design capture rules (col. 1, ll. 44-63, col. 9, ll. 16-36).

9. Pursuant to claim 6, further comprising using a set of abstractions (col. 7, ll. 4-13).

10. Pursuant to claim 10, further comprising generating synthesizable Verilog from the unified database (col. 13, line 40 to col. 14, line 17).

11. Pursuant to claim 11, which recites [a]n article comprising a machine-readable medium which stores executable instructions to generate a logic design for use in designing an integrated circuit (IC) (Fig. 16 illustrates these limitations); the instructions causing a machine to: embed a combinatorial one-dimensional logic block representing a combinatorial element within a two-dimensional schematic representation of the logic design to produce a unified database representation of the logic design (col. 26, ll. 4-16).

12. Pursuant to claims 12 and 22, these claims address limitations already rejected in claim 2, supra, and are likewise rejected here based on similar reasoning.

13. Pursuant to claims 13 and 23, these claims address limitations already rejected in claim 4, supra, and are likewise rejected here based on similar reasoning.

14. Pursuant to claims 14 and 24, these claims address limitations already rejected in claim 3, supra, and are likewise rejected here based on similar reasoning.

15. Pursuant to claim 21 which recites [a]n apparatus for generating a logic design for use in designing an integrated circuit, comprising a memory that stores executable instructions; and a processor that executes the instructions to (Fig. 16 illustrates these limitations): embed a combinatorial one-dimensional logic block representing a combinatorial element within a two-dimensional schematic representation of the logic design to produce a unified database representation of the logic design.

16. Pursuant to claims 15, 16, 20 and 25, 26, 30, these claims address limitations already rejected in claims 5, 6, and 9, respectively, and therefore claims 15, 16, 20 and 25, 26, 30 are likewise respectively rejected here based on similar reasoning.

Allowable Subject Matter

17. Claims 7-9, 17-19, 27-29 are objected to as being dependent upon a rejected base claim, but would be allowable if any existing objections are obviated and the claims are rewritten in independent form including all of the limitations of the base claim and any intervening claims.

18. The following is a statement of reasons for the indication of allowable subject matter: Pursuant to Applicants' method of generating a logic design, the prior art does

not teach generating C++ and Verilog from a unified database. Additionally, the prior art does not teach the inclusion of Register Transfer Diagrams.

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Please reference the PTO-892 for a complete listing.

20. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to A.M. Thompson whose telephone number is (703) 305-7441. The Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 5:00 p.m.. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matthew S. Smith, can be reached on (703) 308-1323.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956 or the Customer Service Center whose telephone number is (703)306-3329.

21. Responses to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9318, (for **OFFICIAL** communications intended for entry)
(703)872-9319, (for Official **AFTER-FINAL** communications)

Hand-delivered responses should be brought to Crystal Plaza 4, 2021 South Clark Place, Arlington, VA., Fourth Floor (Receptionist).

A. M. THOMPSON
Patent Examiner

23 March 2003